REMARKS

The Final Office Action mailed July 26, 2007, has been received and reviewed. Claims 1 through 6, 9 through 15 and 64 are currently pending in the application. Claims 1 through 6, 9 through 15 and 64 stand rejected. No claims are amended herein. Reconsideration is respectfully requested.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,847,461 to Xu et al.

Claims 1 through 6, 9 through 15, and 64 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Xu et al.(U.S. Patent No. 5,847,461, hereinafter Xu '461) in view of Xu et al. (U.S. Patent No. 6,217,721, hereinafter Xu '721) and Yim (U.S. Patent No. 5,869,395). Applicants respectfully traverse this rejection, as hereinafter set forth.

To establish a *prima facie* case of obviousness the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. *In re Royka*, 490 F.2d 981, 985 (CCPA 1974); *see also* MPEP § 2143.03. Additionally, there must be "a reason that would have prompted a person of ordinary skill in the relevant field to combine the [prior art] elements" in the manner claimed. *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1742, 167 L.Ed.2d 705, 75 USLW 4289, 82 U.S.P.Q.2d 1385 (2007). To establish a *prima facie* case of obviousness there must be a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). Furthermore, the reason that would have prompted the combination and the reasonable expectation of success must be found in the prior art, common knowledge, or the nature of the problem itself, and not based on the Applicant's disclosure. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1367 (Fed. Cir. 2006); MPEP § 2144. Underlying the obvious determination is the fact that statutorily prohibited hindsight cannot be used. *KSR*, 127 S.Ct. at 1742; *DyStar*, 464 F.3d at 1367.

Xu '461 teaches an integrated circuit structure having an insulating layer 10 formed over integrated circuit structure 2. Openings 14 and 16 are formed in insulating layer 10 and extend downwardly from upper surface 12 of the insulating layer 10 to expose surfaces 4 and 6 of integrated circuit structure 2 at the bottom of the openings 14 and 16. A barrier layer 20 is

formed over upper surface 12 and insulating layer 10 as well as over the side walls of openings 14 and 16 and over exposed surfaces 4 and 6 at the respective bottoms of openings 14 and 16 (Xu '461, col. 3, lines 12-22). A metal layer 30 comprising a layer of compressively stressed metal is subsequently extruded down into openings 14 and 16 (*Id.*, co. 4, lines 17-23). A cap layer 40 is formed over is formed over metal layer 30. The cap layer 40 of compressively stressed metal is formed over metal layer 30. The cap layer 40 comprises a high tensile strength material to restrain the upward movement of metal layer 30 during the subsequent extrusion step. (*Id.*, col. 6, lines 26-34).

Xu '461 teaches that seed layers are undesirable when filling small openings and is directed toward other methods of filling the contact openings. (*Id.*, col. 1, line 56 – col. 2, line 27). The Examiner acknowledges that Xu '461 fails to teach or suggest a seed layer. (Office Action mailed March 20, 2006, page 7). While Xu '461 focuses on the limitations of tungsten as a seed layer, its teaching that that seed layers add "further deposition and planarization steps, resulting in more cost, and less reliability" would apply to seed layers generally. (*Id.*, col. 2, lines 7-9). Thus, Xu '461 proposes a method to "fill very small diameter openings in an insulating layer with metal such [as] aluminum **initially deposited on the surface of the insulating layer**." (*Id.*, col. 2, lines 19-22, emphasis added).

Yim discloses a method of creating interconnects, but fails to teach or suggest using a seed layer.

Xu '721 teaches an alternative method of filling contact holes 140. A PVD process is used to coat a liner layer 152 onto the sides of a contact hole 140. The liner layer 152 may include a first sublayer 160 of titanium silicide, a second sublayer of titanium nitride 162 and a third sublayer of titanium 164 (deposited as titanium nitride). (Xu '721, col. 12, line 50 – col. 13, line 6; FIG. 8). Standard PVD then deposits a metal layer 156 over the third sublayer 164.

Xu '461, Xu '721 and Yim fail to teach or suggest all the claim limitations of the presently claimed invention. Further, the Examiner has not identified a reason that would have prompted a person of ordinary skill in the relevant field to combine the prior art elements in the manner claimed. The Examiner is using hindsight reconstruction to pick and choose elements from the references to recreate the claimed elements.

Claim 1 of the presently claimed invention recites a "method for manufacturing an interconnect structure consisting essentially of: forming a recess within a dielectric material situated on a semiconductor substrate, the recess extending below a top surface of the dielectric material; forming a diffusion barrier layer substantially conformally on the top surface of the dielectric material and over an interior surface of the recess; forming a seed layer on the diffusion barrier layer over the top surface of the dielectric material and within the recess, the diffusion barrier layer comprising a material having a melting point greater than or equal to that of a material comprising the seed layer, wherein the material comprising the seed layer consists of aluminum, titanium nitride, titanium, or titanium aluminide; forming an electrically conductive layer on the seed layer over the top surface of the dielectric material and substantially within the recess such that voids are present within the recess, the material comprising the diffusion barrier layer having a melting point greater than that of a material comprising the electrically conductive layer, the material comprising the seed layer having a melting point greater than or equal to that of the material comprising the electrically conductive layer; forming an energy absorbing layer on the electrically conductive layer, the energy absorbing layer having a greater thermal absorption capacity than that of the electrically conductive layer; applying energy to the energy absorbing layer sufficient to cause the electrically conductive layer to fill the voids within the recess; and removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material." Applicant respectfully submits that the proposed combination of references fail to teach or suggest every element of the presently claimed invention.

As acknowledged by the Examiner, Xu '461 does not teach or suggest the limitations of "forming a seed layer on the diffusion barrier layer over the top surface of the dielectric material and within the recess, the diffusion barrier layer comprising a material having a melting point greater than or equal to that of a material comprising the seed layer, wherein the material comprising the seed layer consists of aluminum, titanium nitride, titanium, or titanium aluminide" and "forming an electrically conductive layer on the seed layer over the top surface of the dielectric material and substantially within the recess such that voids are present within the recess, the material comprising the diffusion barrier layer having a melting point greater than that

of a material comprising the electrically conductive layer, the material comprising the seed layer having a melting point greater than or equal to that of the material comprising the electrically conductive layer." Therefore, the Examiner relies on Xu '721 as teaching these limitations.

However, Applicant respectfully submits that nothing in the cited references, when combined, suggests the desirability of the combination, or provides an objective reason to combine the teachings of the references. Specifically, nothing in Xu '461 suggests forming a seed layer, let alone forming a seed layer that consists of aluminum, titanium nitride, titanium, or titanium aluminide. Furthermore, the barrier layer in Xu '461 is formed on the insulating layer and the metal layer 30 is formed on the barrier layer. Therefore, Xu '461 does not teach or suggest forming a seed layer on the diffusion barrier layer. Xu '721 also does not teach or suggest forming a seed layer on the diffusion barrier layer. Rather, the TiN_x layer 164 is formed on the second sublayer of the titanium compound, which is itself formed on the first sublayer of titanium.

Applicant disagrees that one would be motivated to substitute the titanium nitride layer 20 of Xu '461 with the titanium/titanium nitride layer 164 of Xu '761. Xu '461 clearly teaches away from a seed layer. (Xu '461, col. 1, line 55- col. 2, line 27). While Xu '461 only specifically mentions tungsten seed layers, tungsten is clearly discussed as an example and generally discloses the problems with seed layers. One skilled in the art would not be motivated to introduce a seed layer on the diffusion barrier layer of Xu '461.

The Examiner states that "it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a seed layer after the formation of the barrier layer and prior to the formation of the conductive layer, and having the thermal properties as taught by Xu '721 in the interconnect method of Xu '461, since heating the barrier layer in a nitrogen environment substantially reduces the electronic barrier at the metal-semiconductor interface . . . and the addition of titanium nitride as a seed layer improves the flow of aluminum into an interconnect at moderate temperatures." Office Action of July 26, 2007, p. 4. However, even assuming *arguendo* that the Examiner's motivation is true, the claimed invention still would not be produced by the combination because the above-mentioned limitations would not be taught or suggested. Specifically, any resulting seed layer would not consist of aluminum, titanium nitride,

titanium, or titanium aluminide and would not be formed on the diffusion barrier layer over the top surface of the dielectric material and substantially within the recess such that voids are present within the recess.

Applicant respectfully submits that Xu '461, Xu '721 and Yim fail to teach or suggest "forming an electrically conductive layer on the seed layer over the top surface of the dielectric material and substantially within the recess such that voids are present within the recess" as recited in claim 1 of the presently claimed invention. The Examiner acknowledges that Xu '461 fails to teach or suggest this claim element. (July 26, 2007, Office Action, page 3). Xu '721 cannot cure the deficiencies of Xu '461 as it lacks any teaching or suggestion of forming an electrically conductive layer . . . such that voids are present within the recess" as recited in claim 1 of the presently claimed invention. Yim fails to cure the deficiencies of Xu '461 and Xu '721.

The Office Action is silent as to *why* one of skill in the art would be motivated to modify Xu '461 to include the missing claim elements. Xu '461 teaches that the initial aluminum layer 30 does not extend within the recess. (FIG. 2) Xu '721 discloses completely filling the via by a PVD process. Thus, assuming the liner layers 152 of Xu '721 could be incorporated into the structure of Xu '461, which applicants do not concede, no reason would exist to fill the via by applying heat and extruding the metal as disclosed in Xu '461. The two Xu references teach alternative methods of filling a contact structure and no motivation exists to combine portions of the first method (i.e., Xu '461) with a second distinct method (i.e., Xu '721).

The cited references also do not teach or suggest the limitation of "removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material." Nothing in Xu '461 teaches or suggests this limitation because, as shown in FIG. 4, the metal layer and the cap layer remain on the integrated circuit structure. Xu '721 also does not teach or suggest removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material. While Yim arguably teaches this limitation, Xu '461 teaches away from this limitation because the same metal is used as the filler in the openings and as the electrically conductive interconnect or wiring harness. Therefore, if portions of the metal layer above the top surface of the dielectric material were removed, as asserted by the Examiner, the resulting structure in Xu

'461 would not have the same metal functioning as the filler in the openings and forming the electrically conductive interconnect or wiring harness.

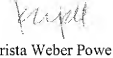
The Examiner has not identified any problem to be solved in Xu '461 that would lead one of skill in the art to modify the method to include the claim elements of claim 1 of the presently claimed invention. The Examiner's statement that it would be obvious to modify Xu '461 to include the elements of claim 1 is merely a conclusion based on a hindsight reconstruction of the claimed invention based on Applicant's own disclosure. As the proposed combination of references fail to teach or suggest every element of independent claim 1 of the presently claimed invention, the proposed combination of references cannot render independent claim 1 of the presently claimed invention obvious. Thus, claim 1 is allowable.

Claims 2- 6, 9 – 15 and 64 are each allowable as depending, either directly or indirectly, from allowable claim 1.

CONCLUSION

Claims 1 through 6, 9 through 15, and 64 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



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